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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,014	04/09/2004	Daniel J. Driscoll	NVDA P001196	1683

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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 04/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/822,014	DRISCOLL ET AL.
	Examiner	Art Unit
	John B. Vigushin	2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,21 and 32-34* is/are rejected.

7)☒ Claim(s) *2-20 and 22-31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1005//11 Oct 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

On p.4, paragraph [0024], "xx/xxx,xxx" needs to be replaced with the appropriate US Application Serial Number.

On p.5, paragraph [0026], "xx/xxx,xxx" needs to be replaced with the appropriate US Application Serial Number.

On p.7, paragraph [0034], the concept of "zero-height regions" is introduced and followed by the bold-emphasized annotation "**[Note: what is meant by 'zero-height' if max height is listed as 3.5 mm?]**". Good question. And it needs to be answered and accompanied by the appropriate deletion or addition of language in paragraph [0034] without creating new matter. Possible guidance for amendment may be found in paragraph [0051] on p.11, for example. Perhaps the term "zero-height" is just a typographical error that should have been rendered as 'z-height', wherein z is a non-zero height value.

On p.12, paragraph [0055], "xx/xxx,xxx" needs to be replaced with the appropriate US Application Serial Number.

Appropriate correction is required.

Rejections Based On Prior Art

2. The following six references were relied upon for the rejections hereinbelow:

Rhoads (US 6,731,515 B2) Bhakta et al. (US 6,222,739 B1)

Evans (US 6,731,514 B2) Mostafazadeh (US 5,783,870)

Corisis et al. (US 6,331,939 B1) Dewey et al. (US 2004/0012082 A1)

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> **(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.**

4. Claim 32 is rejected under 35 U.S.C. 102(e) as being anticipated by Evans.

As to Claim 32, Evans discloses a field changeable card for use in a computer (col.1: 6-15) comprising: a PCB M0 (Figs. 1, 2 and 3; col.3: 9-12 and 60-63); a plurality of mechanical keep-out zones defined on the PCB, the keep-out zones being adapted to accommodate a plurality of on-board components (Figs. 1 and 2), such as the zones corresponding to the support holes 4 for support pillars 8 (col.3: 15-18) and the connector space clearance component 12 (col.3: 18-20 and 54-57), respectively; a card connector zone (corresponding to card connector 14; col.3: 21-23) disposed along a first edge of the PCB (Fig. 2); one or more support holes 4 disposed proximate to a second edge of PCB M0, wherein the second edge is located opposite the first edge and the support holes are sized to receive supports 8 adapted for maintaining the field changeable card in a substantially parallel, spaced apart orientation relative to a

motherboard 50 (Figs. 1 and 3; col.3: 15-18; col.3: 60-col.4: 13), wherein the field changeable card resides in an independent, spaced-apart position relative to motherboard 50 (Fig. 3).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Evans in view of Rhoads and Mostafazadeh et al.

I. Evans discloses a field changeable card for use in a computer (col.1: 6-15) comprising: a PCB M0 (Figs. 1, 2 and 3; col.3: 9-12 and 60-63); a plurality of mechanical keep-out zones defined on the PCB, the keep-out zones being adapted to

accommodate a plurality of on-board components (Figs. 1 and 2), such as the zones corresponding to the support holes 4 for support pillars 8 (col.3: 15-18) and the connector space clearance component 12 (col.3: 18-20 and 54-57), respectively; a card connector zone (corresponding to card connector 14; col.3: 21-23) disposed along a first edge of the PCB (Fig. 2); one or more support holes 4 disposed proximate to a second edge of PCB M0, wherein the second edge is located opposite the first edge and the support holes are sized to receive supports 8 adapted for maintaining the field changeable card in a substantially parallel, spaced apart orientation relative to a motherboard 50 (Figs. 1 and 3; col.3: 15-18; col.3: 60-col.4: 13), wherein the field changeable card resides in an independent, spaced-apart position relative to motherboard 50 (Fig. 3).

II. Evans discloses that the stacked assembly of field changeable cards M0, M1 and motherboard 50 exchange digitally encoded audio, video and other information (col.4: 14-22) such as teletext, program guides and channel information (col.1: 51-56) but does not teach that the field changeable card is a graphics card.

IIIa. Rhoads discloses that the configuration of motherboards with connector slots and circuitry that receive peripheral cards which provide enhanced graphic functions, as well as network interface and audio functions, is old and well-known in the art (col.1: 41-55).

IIIb. Mostafazadeh et al. discloses that the functional packages may be include integrated circuits with microprocessor and graphical functions, among other functions, and may be stacked to utilize less PCB space for a more compact package and

requiring less wiring to reduce parasitic inductances and capacitances, thereby improving electronic performance (col.5: 43-55 and Abstract).

IV. Since Evans discloses the stacked module of field changeable cards M0, M1 includes various functions, among which are graphics, and Rhoads and Mostafazadeh et al. disclose that the cards carry integrated circuits with those functions, then the use of an graphics IC card would have been readily recognized for, at the very least, the type of graphics disclosed in the pertinent art of Evans, as well as other user-required graphics functions for the electronic system, as taught by Rhoads and Mostafazadeh et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the stacked module of Evans with a card M0 that includes a graphics IC in order to perform the teletext graphics and any other graphics applications required in the electronic system to serve the needs of the user of said electronic system, as taught by Rhoads and Mostafazadeh et al.

8. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Evans in view of Rhoads, Mostafazadeh et al. and Bhakta et al.

I. Evans discloses, in Figs. 1, 2 and 3, a computing device comprising a motherboard 50 adapted for receiving a central processing unit 40, and a field changeable card M0 interfaced to the motherboard 50 and residing in an independent, spaced-apart relation to the motherboard 50, the field changeable card comprising: a PCB M0 (Figs. 1, 2 and 3; col.1: 6-15; col.3: 9-12 and 60-63); a plurality of mechanical keep-out zones defined on the PCB, the keep-out zones being adapted to

accommodate a plurality of on-board components (Figs. 1 and 2), such as the zones corresponding to the support holes 4 for support pillars 8 (col.3: 15-18) and the connector space clearance component 12 (col.3: 18-20 and 54-57), respectively; a card connector zone (corresponding to card connector 14; col.3: 21-23) disposed along a first edge of the PCB (Fig. 2); one or more support holes 4 disposed proximate to a second edge of PCB M0, wherein the second edge is located opposite the first edge and the support holes are sized to receive supports 8 adapted for maintaining the field changeable card in a substantially parallel, spaced apart orientation relative to a motherboard 50 (Figs. 1 and 3; col.3: 15-18; col.3: 60-col.4: 13).

IIa. Evans discloses that the stacked assembly of field changeable expansion cards M0, M1 and motherboard 50 exchange digitally encoded audio, video and other information (col.4: 14-22) such as teletext, program guides and channel information (col.1: 51-56) but does not teach that the field changeable card is a graphics card.

IIb. Rhoads discloses that the configuration of motherboards with connector slots and circuitry that receive peripheral cards which provide enhanced graphic functions, as well as network interface and audio functions, is old and well-known in the art (col.1: 41-55).

IIc. Mostafazadeh et al. discloses that the functional packages may be include integrated circuits with microprocessor and graphical functions, among other functions, and may be stacked to utilize less PCB space for a more compact package and requiring less wiring to reduce parasitic inductances and capacitances, thereby improving electronic performance (col.5: 43-55 and Abstract).

IId. Since Evans discloses the stacked module of field changeable expansion cards M0, M1 includes various functions, among which are graphics, and Rhoads and Mostafazadeh et al. disclose that the cards carry integrated circuits with those functions, then the use of an graphics IC card would have been readily recognized for, at the very least, the type of graphics disclosed in the pertinent art of Evans, as well as other user-required graphics functions for the electronic system, as taught by Rhoads and Mostafazadeh et al.

IIe. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the stacked module of Evans with a card M0 that includes a graphics IC in order to perform the teletext graphics and any other graphics applications required in the electronic system to serve the needs of the user of said electronic system, as taught by Rhoads and Mostafazadeh et al.

IIIa. Evans does not teach that the computing device is a laptop computing device.

IIIb. Bhakta et al. discloses a stacked card assembly providing expansion cards for a small computing device, wherein the small computing device includes a laptop computing device that also requires compact packaging afforded by the stacked card arrangement and readily connected/disconnected expansion cards for audio, graphics, and other functions, along with optimal electronic performance capability that is further enhanced by the stacked assembly (col.1: 31-43; col.2: 50-56; col.5: 8-17).

IIIc. Since both Evans and Bhakta et al. are in the same art of stacked electronic assembly for meeting compact space and high performance electronic requirements,

then the application of the stacked card assembly to small computing devices such as laptops, as taught by Bhakta et al., would have been readily recognized in the pertinent art of Evans.

IIId. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the stacked assembly of Evans in a small sized computing device, such as a laptop, as taught by Bhakta et al., in order to provide in Evans both high performance capability and easily accessible functional versatility through expansion cards, as taught by Bhakta et al.

9. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Evans in view of Rhoads, Mostafazadeh et al. and Dewey et al.

I. Evans discloses that the stacked assembly of field changeable cards M0, M1 and motherboard 50 exchange digitally encoded audio, video and other information (col.4: 14-22) such as teletext, program guides and channel information (col.1: 51-56) but does not teach that the field changeable card is a graphics card comprising a graphics processing unit.

IIa. Rhoads discloses that the configuration of motherboards with connector slots and circuitry that receive peripheral cards which provide enhanced graphic functions, as well as network interface and audio functions, is old and well-known in the art (col.1: 41-55).

IIb. Mostafazadeh et al. discloses that the functional packages may be include integrated circuits with microprocessor and graphical functions, among other functions, and may be stacked to utilize less PCB space for a more compact package and

requiring less wiring to reduce parasitic inductances and capacitances, thereby improving electronic performance (col.5: 43-55 and Abstract).

IIc. Dewey et al. discloses that integrated circuit graphical processing units (GPU) 101 are acknowledged as fundamental integrated circuits in a computer system (paragraphs [0005] and [0023]) and discloses a package 102 upon which the GPU IC 101 is mounted, the package 102 electrically interfacing with the motherboard PCB 103 (Figs. 1 and 2; paragraph [0023]).

III. Since Evans discloses the stacked module of field changeable cards M0, M1 includes various functions, among which are graphics, and Rhoads and Mostafazadeh et al. disclose that the cards carry integrated circuits with those functions, and Dewey et al. discloses that the graphic ICs include a graphics processor that is central to the graphics functions of the electronic system, then the use of an GPU IC processor card would have been readily recognized for, at the very least, the type of graphics disclosed in the pertinent art of Evans, as well as other user-required graphics functions for the electronic system, as taught by Rhoads, Mostafazadeh et al. and Dewey et al.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the stacked module of Evans with a card M0 that includes a graphics processing unit in order to perform the teletext graphics and any other graphics applications required in the electronic system to serve the needs of the user of said electronic system, as taught by Rhoads, Mostafazadeh et al. and Dewey et al.

10. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Evans in view of Corisis et al.

I. Evans discloses that the stacked assembly of field changeable cards M0, M1 and motherboard 50 exchange digitally encoded audio signals, as well as video and other information (col.4: 14-22), but does not disclose the field changeable card M0, M1 is an audio chip.

II. Corisis et al. discloses that a stacked assembly 10 comprises chip packages 12 that include a packaged audio processor chip 12 (col.7: 27-31) for use in an electronic system.

III. Since Evans teaches audio functions in a stacked assembly of field changeable card packages and Corisis et al. teaches that one of the packages of such a stacked assembly is an audio processor chip for enabling the audio functions for the electronic system, then the use of an audio chip in a card package peripheral device for system function expansion, as taught in Corisis et al., would have been readily recognized in the pertinent art of Evans.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the field changeable card of Evans to be the packaged audio processor chip of Corisis et al. in order to perform the audio functions already taught in Evans, and as taught by Corisis et al.

Allowable Subject Matter

11. Claims 2-20 and 22-31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Creekmore et al. discloses a surface-mount coupling device 120 that mounts a circuit card 122 to and in parallel with a motherboard 22 without the need for designing keep-out or anti-pad zones (Fig. 8; col.1: 39-col.2: 8; col.2: 66-col.3: 5; and col.8: 51-64).

b) Eibl et al. (US 4,969,066) discloses, in Fig. 2, a circuit board connected to another circuit board such that board connectors 6 are on along a first edge and support holes 12--(with support spacers 4 (Fig. 3)--are disposed proximate a second edge opposite to the first edge.

c) Noschese (US 5,575,686) discloses, in Fig. 1, a circuit card 10B connected to a motherboard 10A such that board connectors 22 are on along a first edge and support holes 18 are disposed proximate a second edge opposite to the first edge.

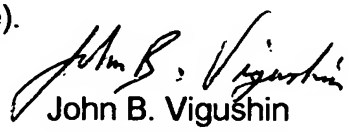
d) Feick (US 4,602,316) discloses, in Fig. 1, a circuit board 12 connected to another circuit board 12 such that board connectors 16 are on along a first edge and support holes 18--with spacer screws 14--are disposed proximate a second edge opposite to the first edge.

e) Furay (US 6,313,984 B1) discloses a portable computer (Fig. 4) comprising a motherboard 36 and disk drive module 50, wherein the disk drive module 50 includes a connector 56 on a first edge and support holes 52 on a second edge opposite to the first edge (Fig. 2).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
April 07, 2006